

a 2<sup>nd</sup> concl.

C

at  
and.

**SECRET**

ad  
cond

---

all  
cont

all  
cancel

the bus clock signal CK frequency and whose phase is shifted by only  $\pi$  through the terminal DATA. In Fig. 7, ABh, CDh, 12h, 34h are hexadecimal numbers. Furthermore, in Fig. 6 and Fig. 7, A1, A2, A3, and A4 are 8-bit data stored in sequence in the trace buffer memory 8.

Replace the paragraph beginning at page 4, line 6 with:

a4  
cancel

However, the processing speed of the microcomputer in the system LSI in recent years is becoming faster and the bus clock frequency therein is increasing. As a result, in the conventional case, access speed to a trace buffer memory cannot catch up with the speed at which data is transmitted from the control circuit. In other words, since one bus cycle is becoming shorter and shorter, it is becoming difficult to store the input data in the trace buffer memory or to output the data from it during one bus cycle.

Replace the paragraph beginning at page 5, line 15 with:

a8  
cancel

Fig. 2 shows time charts of various signals for explaining operation of the first embodiment.

Replace the paragraph beginning at page 5, line 17 with:

a9  
cancel

Fig. 3 shows time charts of various signals for explaining operation of the second embodiment of this invention.

Replace the paragraph beginning at page 5, line 22 with:

a10  
cancel

Fig. 5 shows time charts of various signals for explaining operation of the third embodiment.

Replace the paragraph beginning at page 6, line 1 with:

a11  
cancel

Fig. 7 shows time charts of various signals for explaining operation of the conventional circuit.